What is claimed is:

1. A dual rail bus driver comprising:

a first driver outputting first dual signals of the same level, and outputting second dual signals of different levels when a level of a clock changes;

a decoder receiving the second dual signals and outputting a single signal;

a dual signal controller being triggered due to a change in the level of the second dual signals and outputting third dual signals of different levels in response to the single signal at the same time; and

a second driver inverting the levels of the third dual signals output from the dual signal controller and outputting fourth dual signals in accordance with a change in the level of the clock.

2. The dual rail bus driver of claim 1, wherein the dual signal controller comprises:

a phase change detector detecting changes in the phases of the second dual signals and outputting the detection result as an edge signal; and

an edge trigger flip-flop being triggered by the edge signal and outputting the third dual signals in response to the single signal at the same time.

3. The dual rail bus driver of claim 2, wherein the edge trigger flip-flop is a flip-flop of a sense amplifier type.

4. The dual rail bus driver of claim 1, wherein the second driver is implemented without protective MOS devices.